SYMMETRIC CANCELLING ANTI-STRIATION CIRCUIT

The invention relates to fluorescent lamp driving circuits. More particularly the invention relates to improved techniques for configuring a two-lamp fluorescent lamp for end-of-life detection with an anti-striation circuit.

In the field of fluorescent lamps it is known that some lamps exhibit striations when dimmed to very low levels. One way to remove the striations is to inject a small DC component into a lamp driving current. Some lamps with a small diameter require ballasts having an end-of-life (EOL) detection circuit. A fluorescent lamp tube nearing failure will typically exhibit a fluctuation in impedance that will appear to a detection circuit. As a lamp begins to fail, the EOL circuit senses a change in the DC voltage at the lamp. However, the impedance of a lamp operated at low light output levels is much higher than the lamp impedance of full brightness operation. Therefore, even a small DC current multiplied by the lamp impedance may result in a significant voltage. The EOL circuit cannot distinguish between a lamp voltage due to low-light lamp operation and a voltage change due to an impending lamp failure. An erroneous shut down of the ballast may then be triggered by the EOL sensing circuit. The EOL detection is even less reliable with series connected two lamp configurations, particularly when the lamps have a higher voltage at low dim levels since the lamp voltages will add.

FIG. 1 shows a circuit diagram for an anti-striation circuit for a series-connected two-lamp configuration having end-of-life detection. An isolation transformer T1 couples power to a series connected two-lamp load L1 and L2. A resistor R1 and a diode D1 across the load provide an anti-striation circuit for dimmed operation. A small DC current (Idc), is injected into the load by the voltage drop across R1. A capacitor **C1** senses a change in the potential voltages VL1 and VL2 across the lamps. The scalar impedance of each lamp RL1, RL2, for lamps L1 and L2 respectively is:

$$RL = VL/Idc, \text{ and} \quad (1)$$

the net DC voltage on the capacitor is given by the relationship:

$$VL1 + VL2 = 2*Idc*RL. \quad (2)$$

Generally, the EOL shutdown voltage level must be set higher than the expected DC voltage level resulting from dimmed lamp operation such that:

EOL shutdown DC level > 2*Idc*RL. (3)

It would therefore be desirable to provide an improved anti-striation circuit configuration that addressed these and other limitations.

The present invention is directed to a fluorescent lamp circuit. In accordance with the invention, a power source is selectively arranged to deliver power to a load, a first fluorescent lamp is coupled to the power source and a second fluorescent lamp coupled in series to the first fluorescent lamp and coupled to the power source. A striation correction circuit is coupled to the power source and coupled to the first and second fluorescent lamps. The striation correction circuit is arranged to apply a first striation correction current to the first fluorescent lamp and a second striation correction current to the second fluorescent lamp. A first voltage appearing across the first fluorescent tube due to the first striation correction current is substantially similar in magnitude but has inverted polarity with respect to a second voltage across the second fluorescent tube due to the second striation correction current.

In accordance with another aspect of the invention, a method of reducing striations in a fluorescent lighting circuit is provided. A first striation correction current and a second striation correction current are generated. The first striation correction current is applied to a first fluorescent lamp. The second striation correction current is applied to a second fluorescent lamp. The first fluorescent lamp and the second fluorescent lamp are coupled in series. A first voltage appearing across the first fluorescent lamp due to the first striation correction current is substantially similar in magnitude but has inverted polarity with respect to a second voltage appearing across the second fluorescent lamp due to the second striation correction current.

The foregoing and other features and advantages of the invention are apparent from the following detailed description of exemplary embodiments, read in conjunction with the accompanying drawings. The detailed description and drawings are merely illustrative of the invention rather than limiting, the scope of the invention being defined by the appended claims and equivalents thereof.

FIG. 1 illustrates a prior art anti-striation circuit for a fluorescent lamp ballast having end-of-life detection.

FIG. 2 illustrates a fluorescent lamp circuit having a striation correction circuit and end-of-life detection in accordance with the invention.

FIG. 3 illustrates a second embodiment of the fluorescent lamp circuit of FIG. 2 in accordance with the present invention.

FIG. 4 illustrates another embodiment of a fluorescent lamp circuit as in FIGS. 2 and 3.

FIG. 5 is a flow diagram of a method for reducing striations in a fluorescent lamp system.

In the following description the term "coupled" means either a direct connection between the things that are connected, or a connection through one or more active or passive devices that may or may not be shown, as clarity dictates.

FIG. 2 illustrates a fluorescent lamp circuit having a striation correction circuit and end-of-life detection in accordance with the invention. FIG.2 shows an isolation transformer T1 coupled to a closed-loop circuit comprising: a capacitor C1; a striation correction circuit further comprising a first lamp correction circuit having a diode D1 in series with a resistor R1, and a second lamp correction circuit having a diode D2 in series with a resistor R2; and, first and second series-coupled fluorescent lamps, L1 and L2. The first and second lamp correction circuits are coupled in series with the diodes, D1 and D2, opposing one another in current sense. The first fluorescent lamp L1 is shown in parallel with the first lamp correction circuit, D1 and R1. The second fluorescent lamp L2 is shown in parallel with the second lamp correction circuit, D2 and R2. The capacitor C1 is shown in series with the transformer T1 and the lamp circuits.

Power is selectively coupled to the fluorescent lamp circuit through the transformer T1. A dimmable switch-mode or PWM-type ballast is generally coupled to the transformer T1 primary (not shown). The transformer T1 is typically an isolation transformer and may have one or more taps. The diodes, D1 and D2, are any suitable diodes having a power rating commensurate with the required DC striation correction currents, and typically will have the same rated values within the standard manufacturer tolerance ranges. In one embodiment (not shown), D1 and D2 are transistors configured as diodes. The resistors, R1 and R2, are any suitable resistors for providing a voltage drop to generate a DC current, and generally have the same rated value within standard manufacturing tolerance ranges. The resistors, R1 and R2, are generally metal film types, but carbon and wire wound resistors are interchangeable. In one

embodiment (not shown), R1 and R2 are transistors configured as resistive loads. The fluorescent lamps, L1 and L2, are any suitable fluorescent lamps, typically of narrow diameter and dimmable. The capacitor C1 is any capacitor suitable for sensing a loop DC voltage change (EOL) due to an end-of-life condition on a fluorescent tube. In one embodiment, an EOL detection circuit is coupled to the capacitor C1 (not shown.)

In operation, a DC current Idc is induced in each lamp correction circuit by applying power to the transformer T1 primary. A voltage across the secondary of the transformer T1 causes a voltage drop across resistors R1 and R2. Symmetric DC currents are injected to the fluorescent lamps L1 and L2, due to the orientation of the diodes D1 and D2. As shown in FIG. 2, the current Idc injected to the fluorescent lamps L1 and L2 is substantially equivalent in magnitude within a tolerance range, but opposite in sense. The opposing sense of the injected current Idc causes the resulting DC voltages on the fluorescent lamps, L1 and L2, to be opposite in polarity and therefore substantially eliminated from the loop voltage. Therefore, under normal operation of the fluorescent lamp circuit, the net DC voltage on the capacitor C1 is zero. The shutdown threshold voltage for the EOL sensing circuit may be configured based upon the fluorescent lamp characteristics without regard to the striation correction circuits.

FIG. 3 illustrates a second embodiment of the fluorescent lamp circuit of FIG. 2 in accordance with the present invention. FIG. 3 shows a fluorescent lamp circuit 300 comprising a transformer T4 coupling a ballast circuit 310 to a closed-loop circuit comprising a capacitor C1; a striation correction circuit comprising a first lamp correction circuit having a diode D1 in series with a resistor R1 and a second lamp correction circuit having a diode D2 in series with a resistor R2; first and second series-coupled fluorescent lamps, L1 and L2; and, an EOL detection circuit comprising current sense transformer T5, capacitors C9, C10, and C11 and C12, and, transformers T9, T10, T11. The first and second lamp correction circuits are coupled in series with the diodes, D1 and D2, opposing one another in current sense. The first fluorescent lamp L1 is shown in parallel with the first lamp correction circuit, D1 and R1. The second fluorescent lamp L2 is shown in parallel with the second lamp correction circuit, D2 and R2. The capacitor C1 is shown in series with the transformer T1 and the lamp correction circuits. Capacitor C12 is shown coupled in series to the current

sense transformer T5. Capacitor C9 and transformer T9 are shown in series with the current sense transformer T5 and a first end of the first fluorescent lamp L1. Capacitor C10 and transformer T10 are shown in series with the lamp correction circuits and a second end of the first fluorescent lamp L1 and a first end of the second fluorescent lamp L2. Capacitor C11 and transformer T11 are shown in series with the current sense transformer T5 and a second end of the second fluorescent lamp L2. In one embodiment (not shown), additional components such as current sources, pass transistors and bias resistors are included in fluorescent lamp circuit 300. EOL detection circuits will be known to those skilled in the art and will not be further discussed.

In operation, the fluorescent lamp circuit 300 provides fluorescent lamp striation correction for dimmed operation and reliable end-of-life detection. As in FIG. 2, a DC current Idc is induced in each lamp correction circuit by applying power to the transformer T4 primary. A voltage across the secondary of the transformer T1 causes a voltage drop across resistors R1 and R2. Symmetric DC currents are injected to the fluorescent lamps L1 and L2. The current Idc injected to the fluorescent lamps, L1 and L2, is substantially equivalent in magnitude within a tolerance range, but opposite in sense. The opposing sense of the injected current Idc causes the resulting DC voltages on the fluorescent lamps, L1 and L2, to be opposite in polarity and therefore substantially eliminated from the loop voltage. Therefore, under normal operation of the fluorescent lamp circuit 300, the net DC voltage on the capacitor **C1** is zero. The shutdown threshold voltage for the EOL sensing circuit may be configured based upon the fluorescent lamp characteristics without regard to the striation correction circuits. In one embodiment (not shown), two or more fluorescent lamp circuits 300 may be configured for parallel operation with a combined power source.

FIG. 4 illustrates yet another embodiment of a fluorescent lamp circuit as in FIGS. 2 and 3. In particular, FIG. 4 shows a detailed schematic including an embodiment of a fluorescent lamp circuit as implemented in FIG. 3. A skilled practitioner will recognize components of a standard ballast circuit depicted in FIG. 4. The design and operation of ballast circuits is known to skilled practitioners and therefore the components and operation of the ballast circuit portions of FIG. 4 will not be discussed. Of relevance to the present invention in FIG. 4 is a striation correction

circuit comprising a first lamp correction circuit having a diode D24 in series with a resistor R38 and a second lamp correction circuit having a diode D23 in series with a resistor R38A; an EOL detection circuit comprising current sense transformer T5, capacitors C27, C28, and C29 and, transformers T1-C, T1-8, T1-9. The first and second lamp circuits are coupled in series with the diodes, D24 and D23, opposing one another in current sense. The first fluorescent lamp resides between terminals RED-A - RED-B and YEL-A - YEL-B which is shown in parallel with the first lamp correction circuit, D24 and R38. The second fluorescent lamp resides between terminals YEL-A - YEL-B and BLU-A - BLU-B which is shown in parallel with the second lamp correction circuit, D23 and R38A. The capacitor C25 is shown in series with the transformer T4 and the lamp correction circuits. Capacitor C31 is shown coupled in series to the current sense transformer T5. Capacitor C29 and transformer T1-9 are shown in series with the current sense transformer T5 and a first end of the first fluorescent lamp L1. Capacitor C27 and transformer T1-C are shown in series with the lamp correction circuits and a second end of the first fluorescent lamp L1 and a first end of the second fluorescent lamp L2. Capacitor C26 and transformer T1-9 are shown in series with the current sense transformer T5 and a second end of the second fluorescent lamp L2. Additional components such as current sources, pass transistors and bias resistors included in fluorescent lamp circuit will be understood by the skilled practitioner and will not be discussed.

In the following process description certain steps may be combined, performed simultaneously, or in a different order.

FIG. 5 is a flow diagram of a method for reducing striations in a fluorescent lamp system. Process 500 begins in step 510. In step 510, a first striation correction current and a second striation correction current are generated. The striation correction currents may be created at any time power is applied to the fluorescent lamp system. Generally, the first and second striation correction currents are simultaneously generated responsive to the application of a power source, as in the voltage drop across resistors R1 and R2. The striation correction currents are DC currents of a magnitude that reduces striations in fluorescent lamps operated at low light levels. In one embodiment, generation of the striation correction currents is selectably controlled

based on the operational status of the fluorescent lamp. For instance, detection of an end-of-life condition by an EOL circuit such as described in FIGS. 3 and 4 may trigger a shut down of the striation correction current generation. In another embodiment, generation of the striation correction currents is selectably controlled based on the light output configuration of the lamp. For instance, selection of normal light level lamp operation may trigger a shutdown of striation correction current generation, whereas selection of low light level lamp operation may trigger striation correction current generation.

In step 520, the first striation correction current is applied to a first fluorescent lamp L1. Application of the first striation correction current may occur at any time during or after generation of the correction current. Typically, application of the first striation correction current is concurrent with current generation.

In step 530, the second striation correction current is applied to a second fluorescent lamp L2. Application of the second striation correction current may occur at any time during or after generation. Typically, application of the second striation correction current is concurrent with both generation of the second striation current and generation and application of the first striation correction current. The second striation correction current is applied in an opposite sense to the application of the first striation correction current such that a first voltage appearing across the first fluorescent lamp L1 resulting from the first striation correction current is substantially similar in magnitude and having inverted polarity with respect to a second voltage across the second fluorescent tube L2 resulting from the second striation correction current.

While the preferred embodiments of the invention have been shown and described, numerous variations and alternative embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

CLAIMS:

1. A fluorescent lamp circuit, comprising:

a power source selectively arranged to deliver power to a load;

a first fluorescent lamp coupled to the power source;

a second fluorescent lamp coupled in series to the first fluorescent lamp and coupled to the power source; and

a striation correction circuit coupled to the power source and coupled to the first and second fluorescent lamps that is arranged to apply a first striation correction current to the first fluorescent lamp and a second striation correction current to the second fluorescent lamp wherein a first voltage appearing across the first fluorescent tube resulting from the first striation correction current is substantially similar in magnitude and having inverted polarity with respect to a second voltage across the second fluorescent tube resulting from the second striation correction current.

2. The circuit of claim 1 further comprising an end-of-life detection circuit coupled to the first and second fluorescent lamps.

3. The circuit of claim 2 wherein the end-of-life detection circuit comprises a capacitor arranged in series with the first and second fluorescent lamps to sense voltage changes in a closed-loop circuit with the power source and the first and second fluorescent lamps.

4. The circuit of claim 3 wherein the end-of-life detection circuit further comprises a current sense transformer.

5. The circuit of claim 1 wherein the striation correction circuit comprises a first lamp correction circuit for generating the first striation correction current in the first fluorescent lamp and a second lamp correction circuit for generating the second striation correction current in the second fluorescent lamp.

6. The circuit of claim 5 wherein the first lamp correction circuit is arranged in parallel with the first lamp and the second lamp correction circuit is arranged in parallel with the second lamp and wherein the first and second lamp circuits are in series.

7. The circuit of claim 6 wherein the first lamp correction circuit and the second lamp correction circuit each comprise a diode in series with a resistor and wherein the first and second lamp correction circuits are arranged symmetrically with the diodes opposing one another other.

8. The circuit of claim 5 wherein the first lamp correction circuit and the second lamp correction circuit comprises at least one transistor.

9. The circuit of claim 1 wherein the power source is a fluorescent lamp ballast coupled to the first and second fluorescent lamps through an isolation transformer.

10. The circuit of claim 1 wherein the fluorescent lamp circuit comprises at least one additional pair of fluorescent lamps and at least one additional corresponding striation correction circuit all coupled to the power source and wherein the at least one additional pair of fluorescent lamps are arranged in series with the first and second fluorescent lamps.

11. The circuit of claim 1 wherein the first and second striation correction currents are DC signals and wherein the first striation current is opposite in sense to the second striation current.

12. A method of reducing striations in a fluorescent lighting system, comprising:

generating a first striation correction current and a second striation correction current;

applying the first striation correction current to a first fluorescent lamp; and

applying the second striation correction current to a second fluorescent lamp wherein the first fluorescent lamp and the second fluorescent lamp are coupled in series and wherein a first voltage appearing across the first fluorescent lamp resulting from the first striation correction current is substantially similar in magnitude and having inverted polarity with respect to a second voltage appearing across the second fluorescent lamp resulting from the second striation correction current.

13. The method of claim 12 further comprising:

sensing a voltage change in the fluorescent lighting circuit indicative of a fluorescent tube end-of-life condition wherein an end-of-life detection circuit is coupled to the first and second fluorescent lamps.

14. The method of claim 13 wherein the end-of-life detection circuit comprises a capacitor arranged in series with the first and second fluorescent lamps.

15. The method of claim 12 wherein the striation correction circuit comprises a first lamp correction circuit for generating the first striation correction current in the first fluorescent lamp and a second lamp correction circuit for generating the second striation correction current in the second fluorescent lamp.

16. The method of claim 15 wherein the first lamp correction circuit is arranged in parallel with the first lamp and the second lamp correction circuit is arranged in parallel with the second lamp and wherein the first and second lamp correction circuits are in series.

17. The method of claim 16 wherein the first lamp correction circuit and the second lamp correction circuit each comprise a diode in series with a resistor and wherein the first and second lamp correction circuits are arranged symmetrically with the diodes opposing one another other.

18. The method of claim 16 wherein the first lamp correction circuit and the second lamp correction circuit are comprised of at least one component selected from the group consisting of a transistor, a resistor, a diode, a capacitor and an inductor.

19. The method of claim 12 wherein the fluorescent lamp circuit comprises at least one additional pair of fluorescent lamps and at least one additional corresponding striation correction circuit all coupled to the power source and wherein the at least one additional pair of fluorescent lamps are arranged in series with the first and second fluorescent lamps.

20. A system for reducing striations in a multi-tube fluorescent lamp assembly, comprising:

means for generating a first striation correction current and a second striation correction current;

means for applying the first striation correction current to a first fluorescent lamp;

means for applying the second striation correction current to a second fluorescent lamp; and,

wherein the first fluorescent lamp and the second fluorescent lamp are coupled in series and wherein a first voltage appearing across the first fluorescent lamp resulting from the first striation correction current is substantially equal in magnitude and having inverted polarity with respect to a second voltage appearing across the second fluorescent lamp resulting from the second striation correction current.

ABSTRACT

A striation correction circuit is arranged to apply a first striation correction current to the first fluorescent lamp and a second striation correction current to the second fluorescent lamp. A first voltage appearing across the first fluorescent tube due to the first striation correction current is substantially similar in magnitude but has inverted polarity with respect to a second voltage across the second fluorescent tube due to the second striation correction current. Detection of an end-of-life condition of a fluorescent lamp is thereby facilitated.

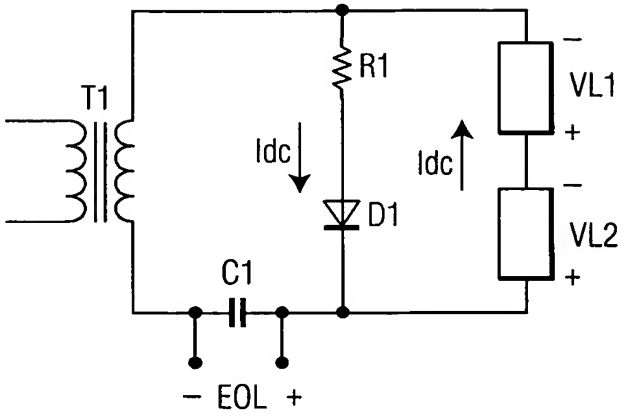


FIG. 1
PRIOR ART

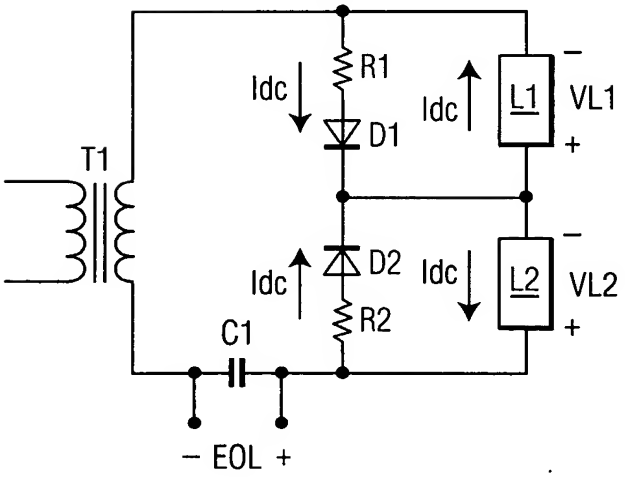


FIG. 2

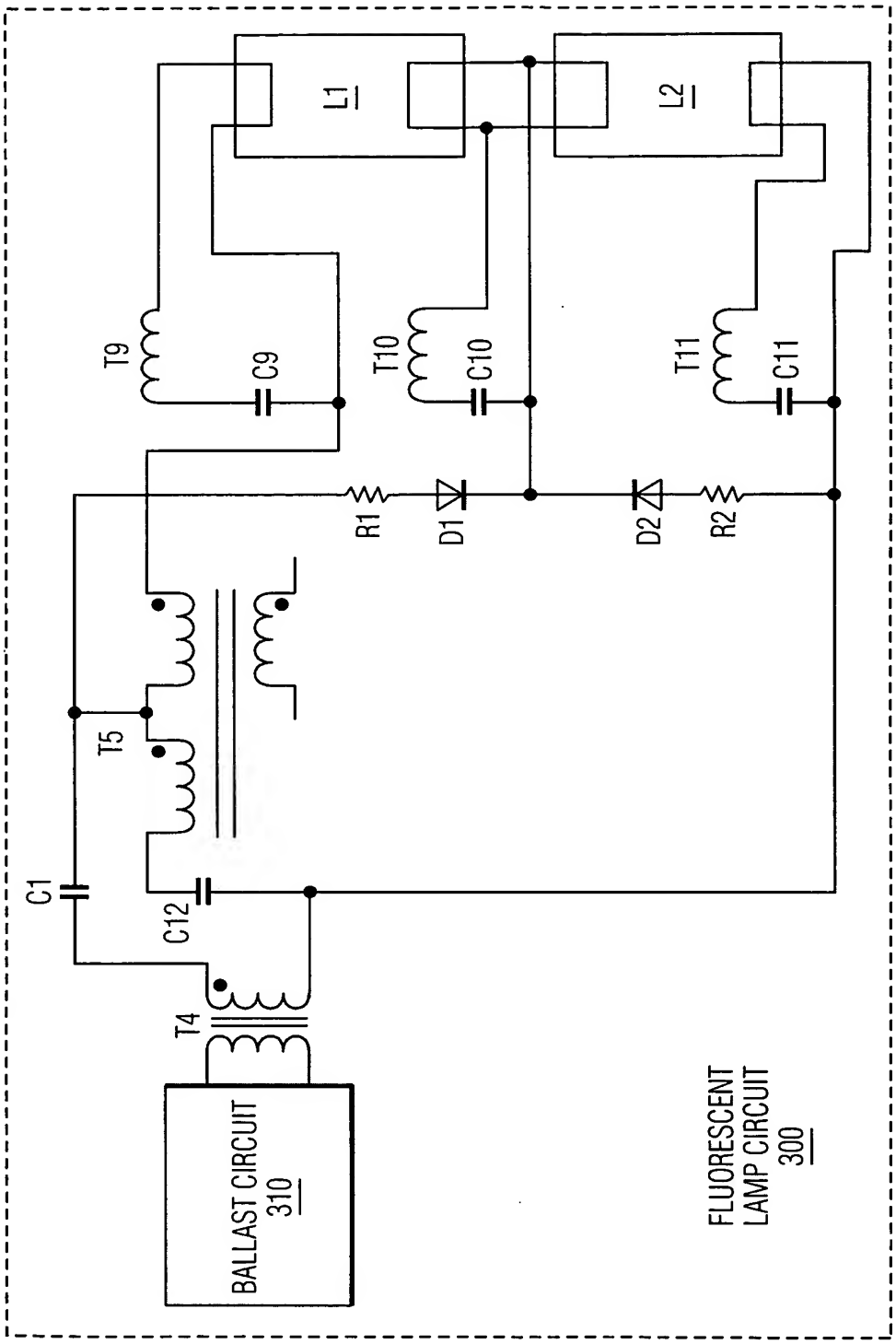
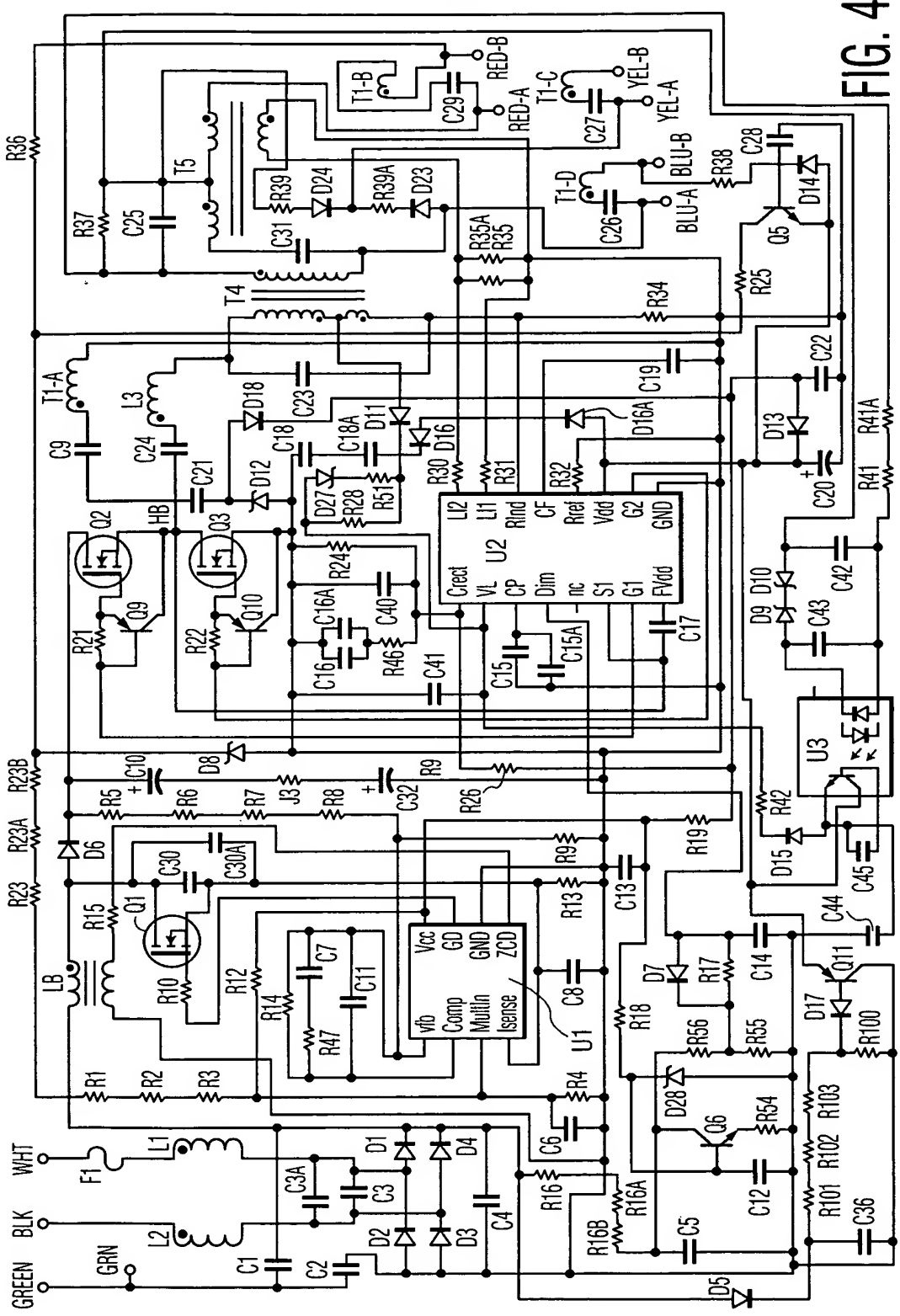

L1
L2
T9
C9
T10
C10
T11
C11
R1
D1
D2
R2
T5
C1
C12
T4
BALLAST CIRCUIT
310
FLUORESCENT
LAMP CIRCUIT
300

FIG. 3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BLK
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GRN
F1
L1
L2
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T1-A
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T4
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U3
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GND
ZCD
Vfb
Comp
Multiln
Isense
Crect
VL
CP
Dim
nc
S1
G1
FVdd
LI2
LI1
Rlnd
CF
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HB
RED-B
RED-A
YEL-B
YEL-A
BLU-B
BLU-A
FIG. 4

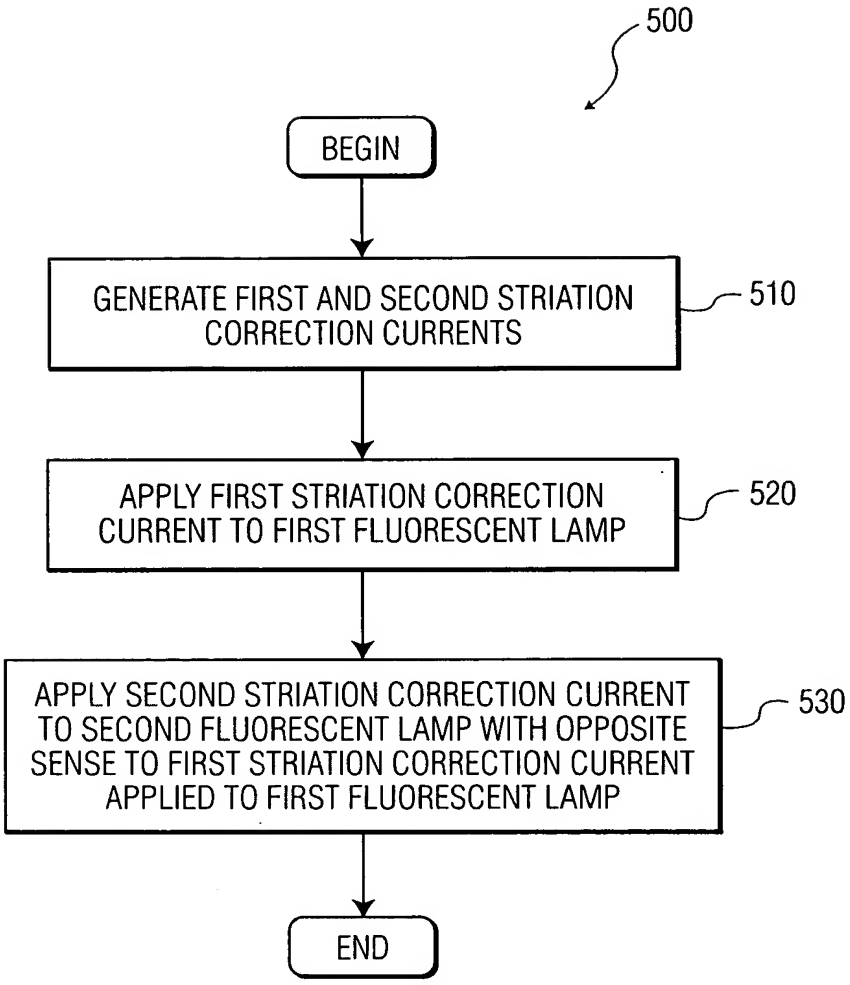
500
BEGIN
GENERATE FIRST AND SECOND STRIATION CORRECTION CURRENTS
510
APPLY FIRST STRIATION CORRECTION CURRENT TO FIRST FLUORESCENT LAMP
520
APPLY SECOND STRIATION CORRECTION CURRENT TO SECOND FLUORESCENT LAMP WITH OPPOSITE SENSE TO FIRST STRIATION CORRECTION CURRENT APPLIED TO FIRST FLUORESCENT LAMP
530
END

FIG. 5

INTERNATIONAL SEARCH REPORT

PCT/IB 03/05228

Rec'd PCT/PTO 25 MAY 2005

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05B41/285

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 701 059 A (STEIGERWALD ROBERT LOUIS ET AL) 23 December 1997 (1997-12-23) column 1, line 12 -column 2, line 2 column 3, line 61 -column 4, line 10; figure 6	1,5-8, 11,12, 15-18,20 2,3,13, 14
Y	WO 97 43879 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 20 November 1997 (1997-11-20) page 6, line 10 -page 7, line 2; figure 1	2,3,13, 14
A	EP 0 547 674 A (KONINKL PHILIPS ELECTRONICS NV) 23 June 1993 (1993-06-23)	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 February 2004	23/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Speiser, P

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